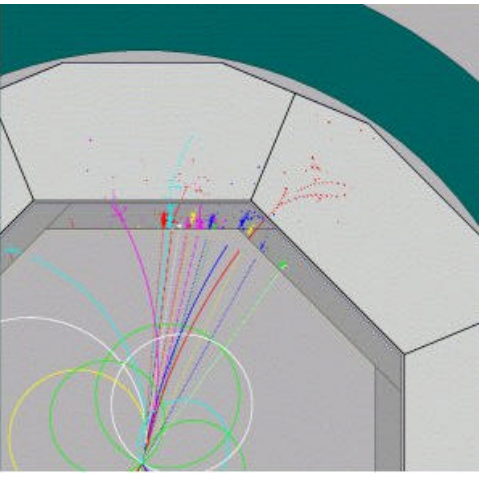


Front-End electronics for Future Linear Collider W-Si calorimeter physics prototype

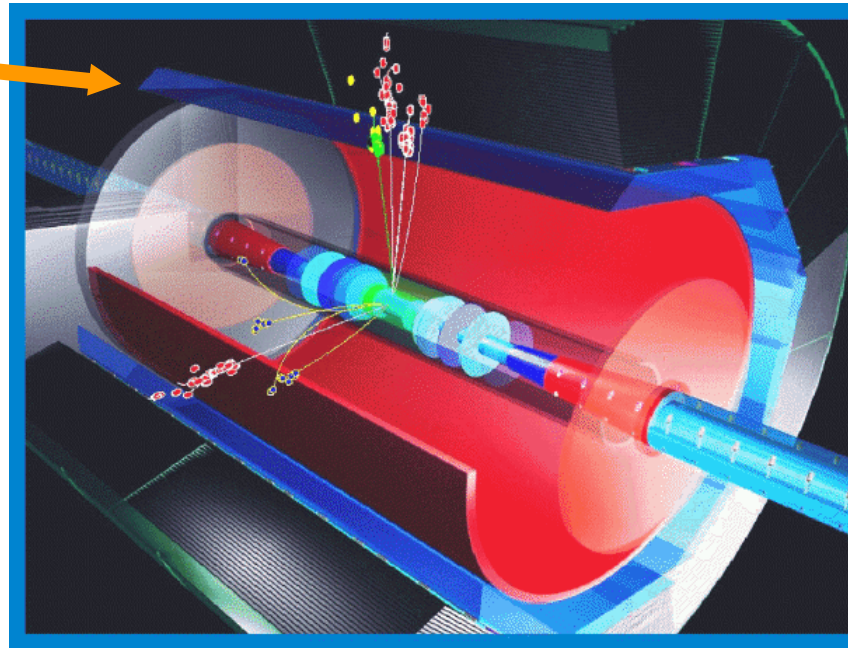
B. Bouquet, J. Fleury, C. de La Taille, G. Martin-Chassard

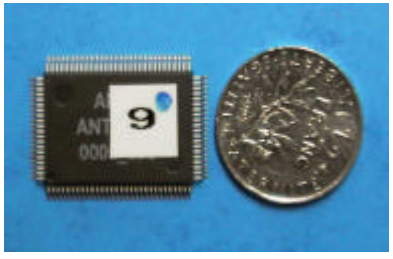
LAL Orsay

http::/www.lal.in2p3.fr/technique/se/flc

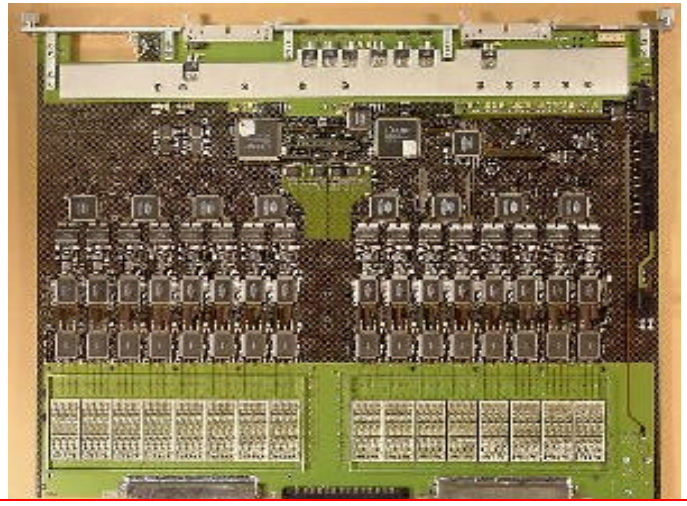
Introduction : FLC challenges for electronics

- **CALICE = W-Si Calorimeter**
  - Precision measurements : ~10%/√E
    - good linearity (‰ level)
    - Good inter-calibration (% level)
    - Low crosstalk (‰ level)
  - Large dynamic range
    - 0.1 MIP -> 2 500 MIPS = 15 bits
  - Low noise
    - Auto-trigger on MIP (40, 000 e-)
  - Hermeticity : no room for electronics !
    - High level of integration : « SoC »
    - Ultra-low power : (≪ mW/ch)
  - 30 Mchannels
- **« Tracker electronics with calorimetric performance »**





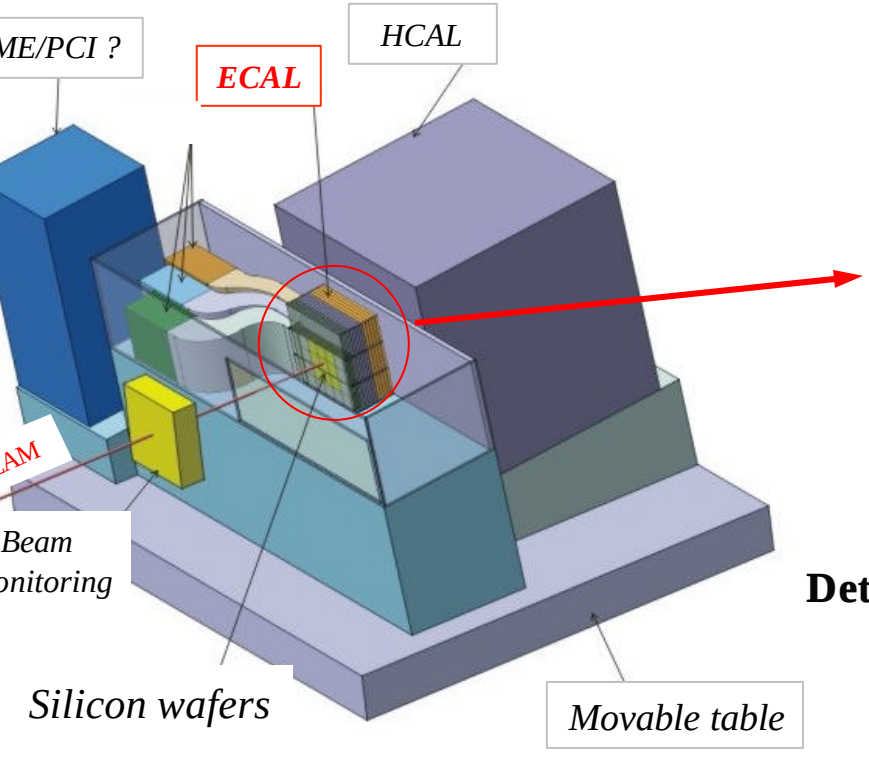
FLC 128ch 30*20mm 1 W ?

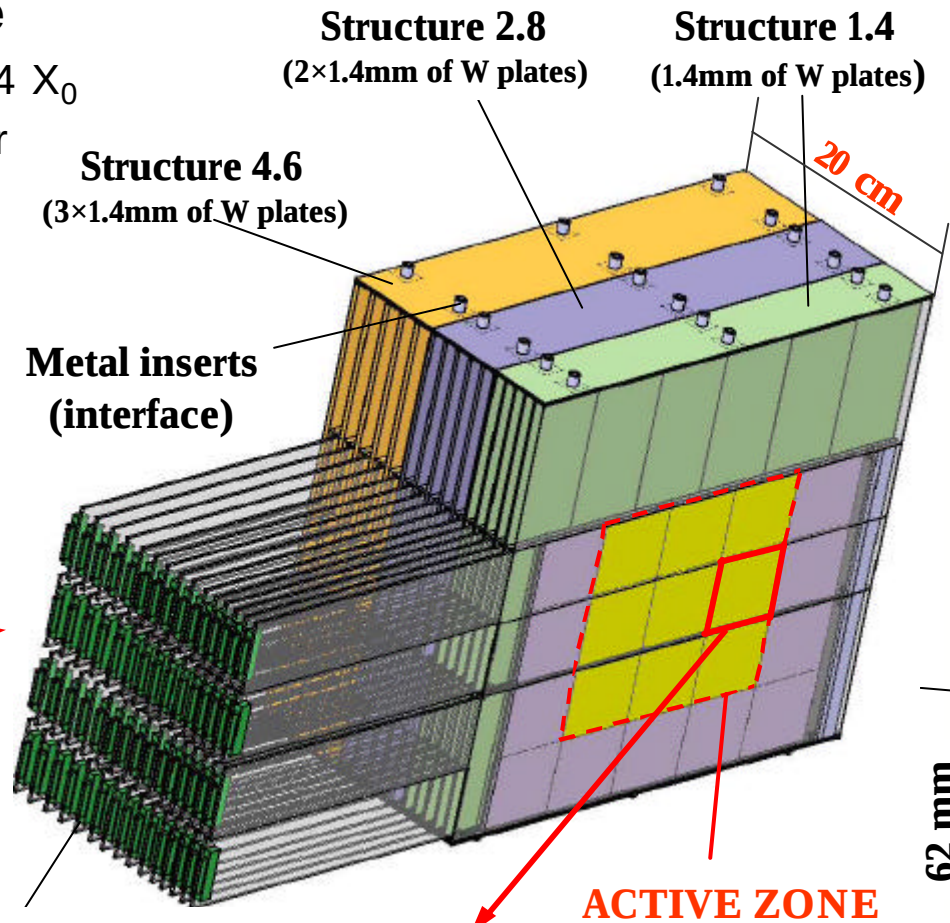


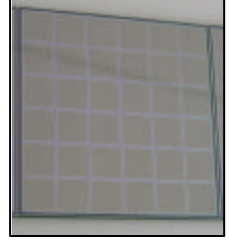
ATLAS LAr FEB 128ch 400*500mm 100 W

Physics prototype overview

- **Multi-layer (30) W-Si prototype**
  - Active area : 18x18 cm^2 ,depth : 24 X_0
  - 30 detector slabs slid into alveolar structure
  - *See talk by J.C Brient*





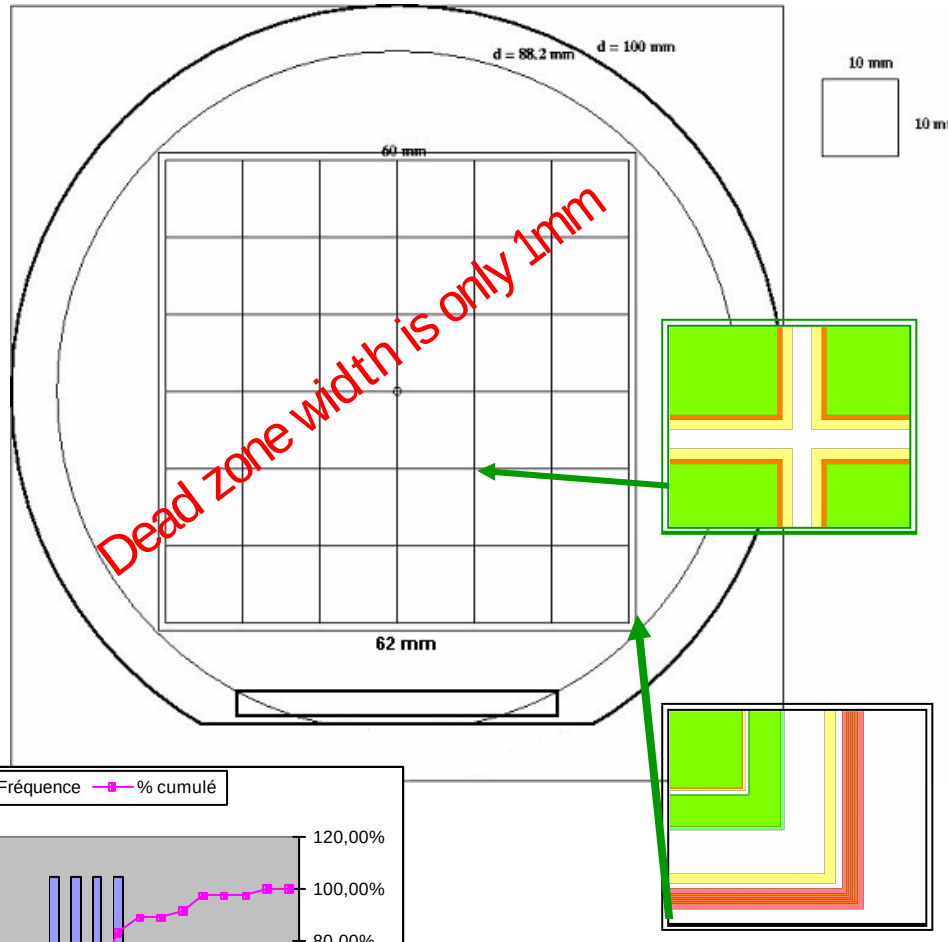


Si wafer
6x6 diodes

Silicon wafer description

[JC Vanel LLR lab]

- **Matrix of 6x6 pixels of 1 cm²**
  - Low cost => simple process
  - 2 manufacturers :
    - INP Moscow
    - Institute of Physics Prague
  - AC coupling on PCB



4" High resistive wafer : 5 KΩcm

Thickness : 525 microns ± 3 %

Tile side : $62.0\ ^{+0}_{-0.1}$mm

Guard ring

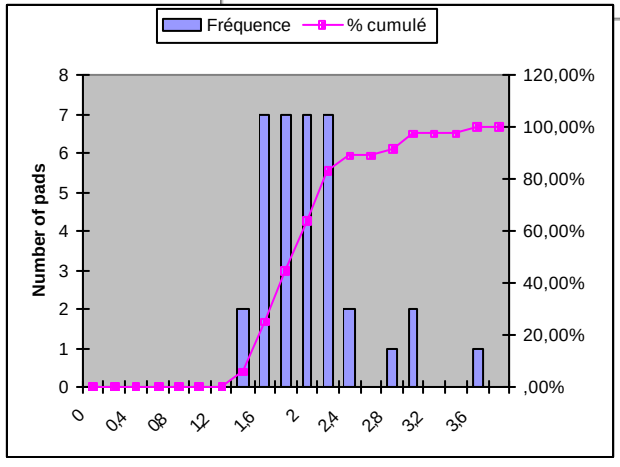
In Silicone ~80 e-h pairs / micron
⇒ 42000 e^- /MiP

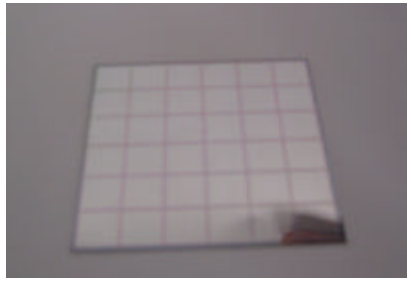
Capacitance : ~25 pF

Leakage current : 1 – 5 nA

Full depletion bias : ~150 V

Nominal operating bias : 200 V





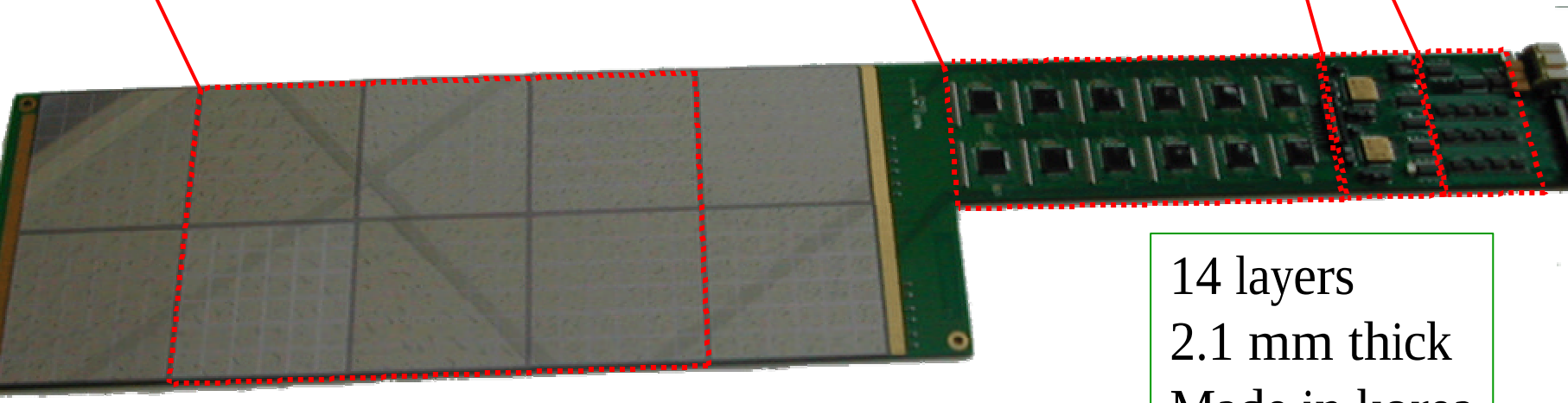
Front-end board

6 active wafers
Made of 36 silicon PIN diodes
216 channels per board
Each diode is a 1cm² square

2 calibration switches chips
6 calibration channels per chip
18 diodes per calibration channel
See talk on ATLAS calibration

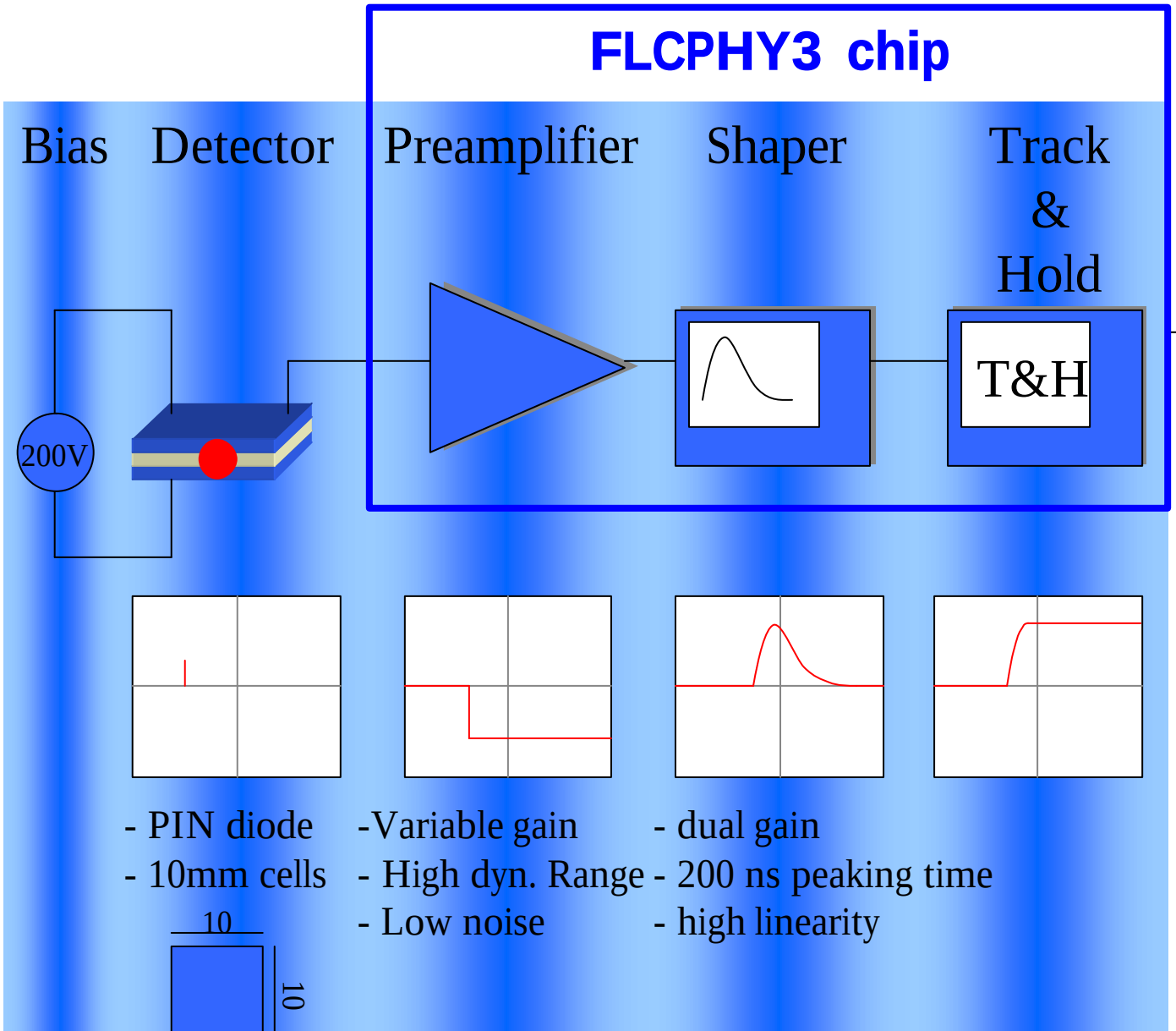
12 FLCPHY3 front-end chip
18 channels per chip
13 bit dynamic range

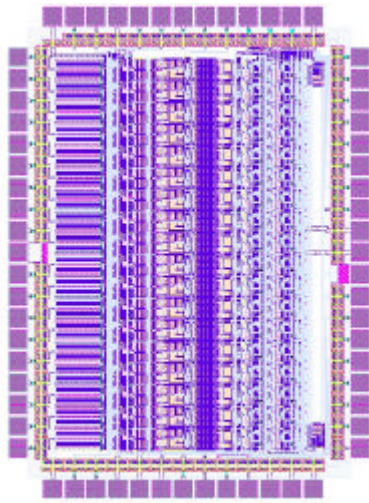
Line buffers
To DAQ part
Differential



14 layers
2.1 mm thick
Made in korea

Front-end electronics synoptic



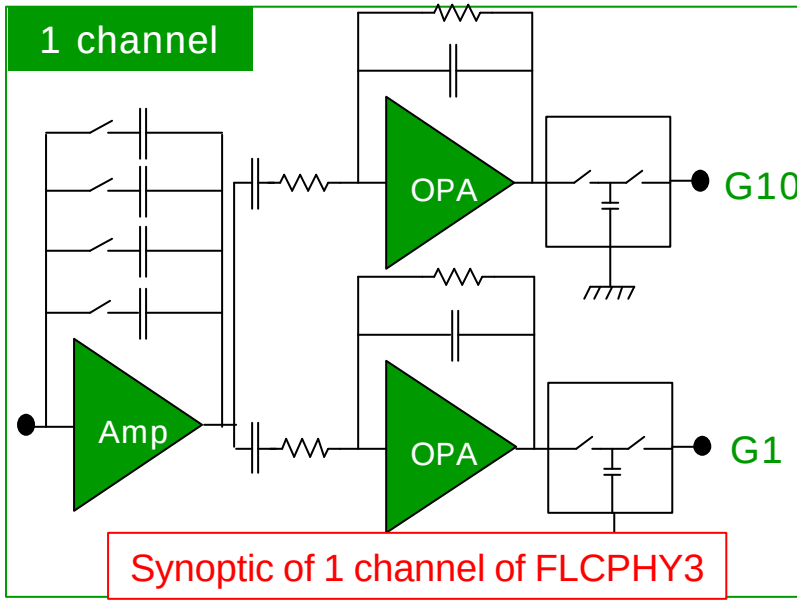


FLCPHY3

- BiCMOS 0.8µm
- 18 channels
- Area : 6 mm2
- V_{SS} = - 5V
- P_d = 250 mW
- TQFP64 packg

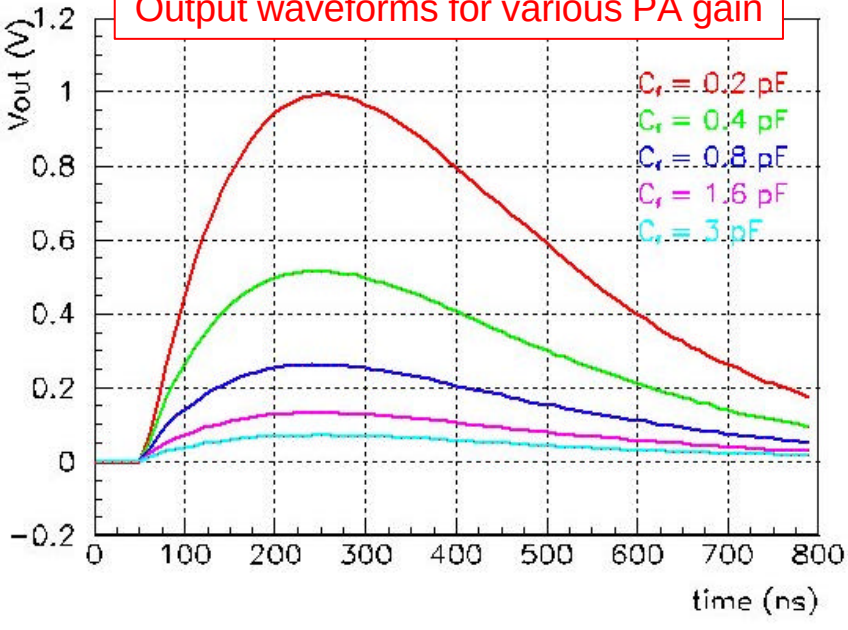
FLCPHY chip architecture

- **Chip architecture**
  - Variable gain preamp (Cf = 0.2 -> 3 pF) adapt to several detectors
  - Dual gain shaper (G1-G10) -> possible studies with larger (16bit) dynamic range
  - Differential shaper and Track&Hold => better pedestal stability and dispersion
  - Multiplexed output : 5 MHz

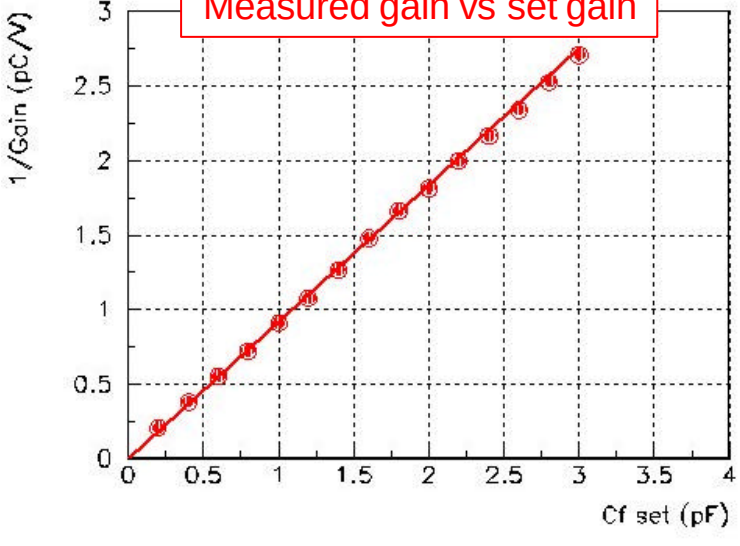


Synoptic of 1 channel of FLCPHY3

Output waveforms for various PA gain



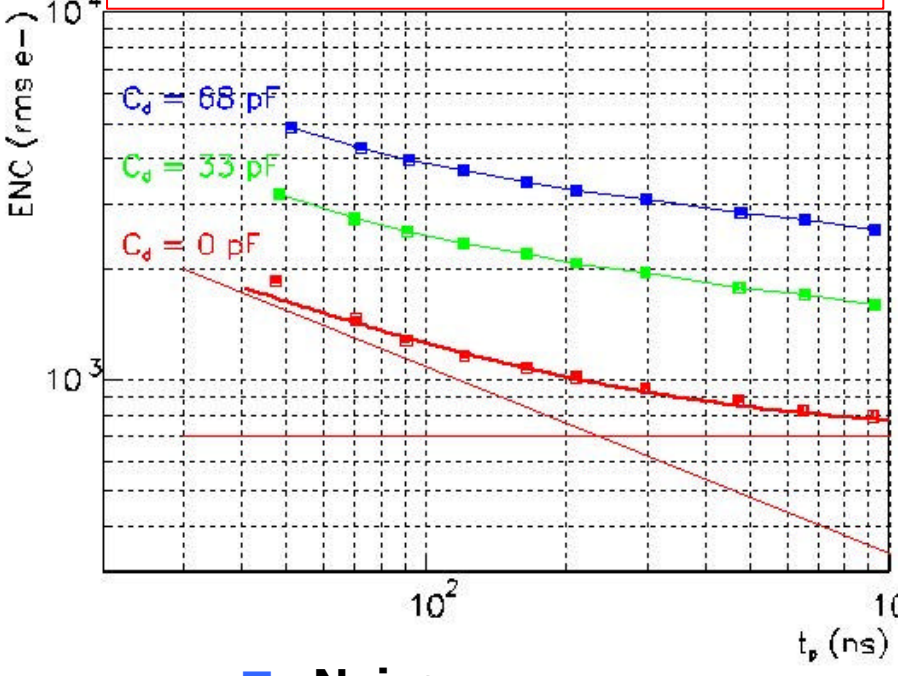
Measured gain vs set gain

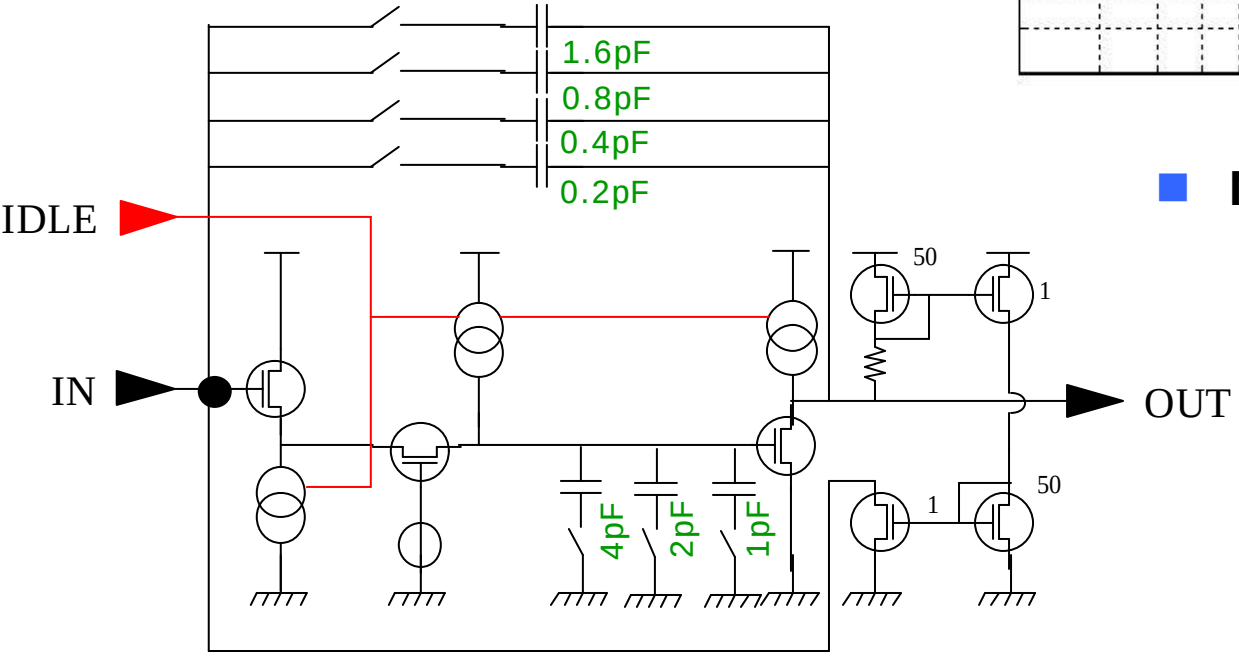


Preamp performance : noise

- **Charge preamp**
  - Folded cascode, negative output
  - « mirror multiplied » feedback resistor, equivalent to 25 MO
  - 3000/0.8µm PMOS input transistor
  - I_D=600 µA bias current, 4mW total
  - ENC = 1000e- + 40 e-/pF @ tp=200ns

ENC measurement of the FLCPHY3 preamp

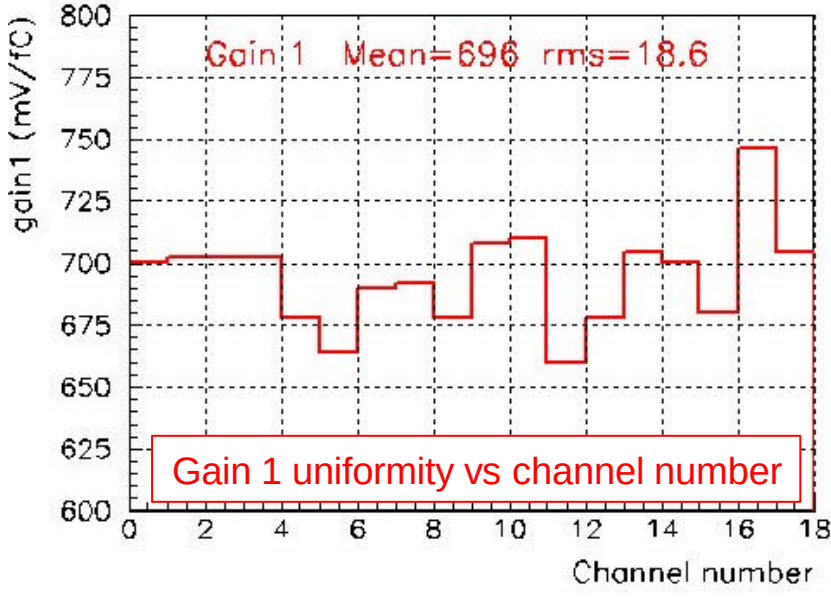


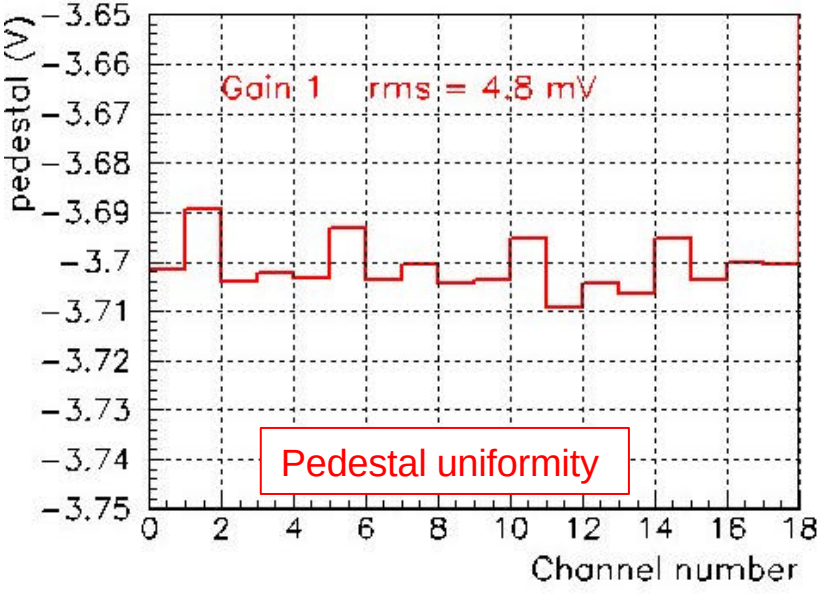


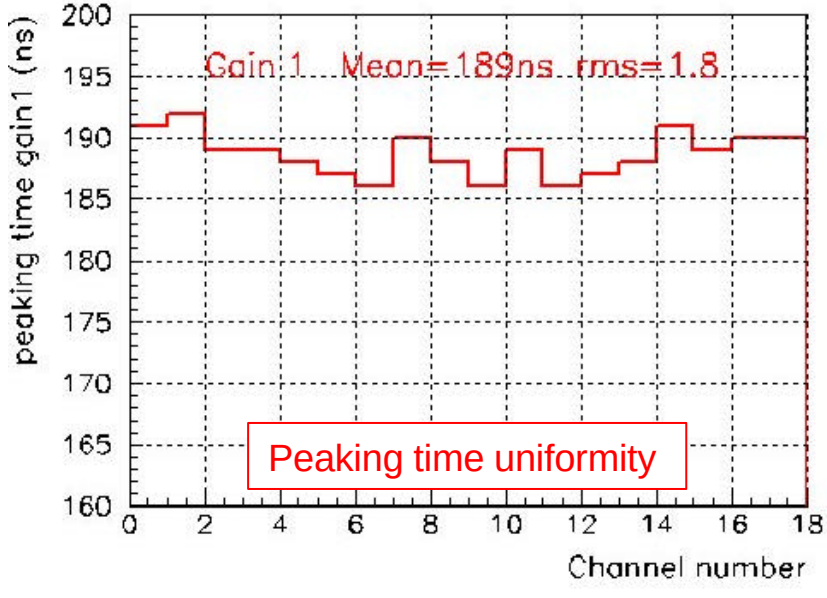
- **Noise**
  - Series : e_n = 1.6nV/vHz
  - g_m= 8 mA/V
  - C_{PA} = 10pF + 15pF test board
  - 1/f noise : 25e-/pF
  - Parallel : i_n = 40 fA/vHz

Signal uniformity (G1)

- **Signal (Gain 1, C_f=1.6pF)**
  - Amplitude = 696 mV/pC ± 18 mV
    = 4.66 mV/ MIP ± 2.5% rms
  - Peaking time = 189 ns ± 2 ns rms
  - Pedestals = -3.7 V ± 4.8 mV rms
- **Noise**
  - Cd = 0 pF : Vn = 200 µV
  - Cd = 68pF : Vn = 410 µV
- **Crosstalk : < 0.1%**

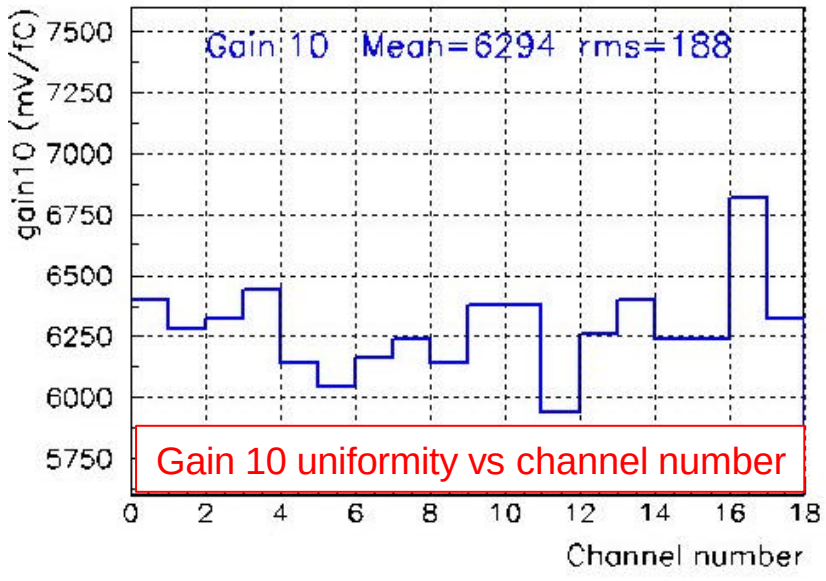


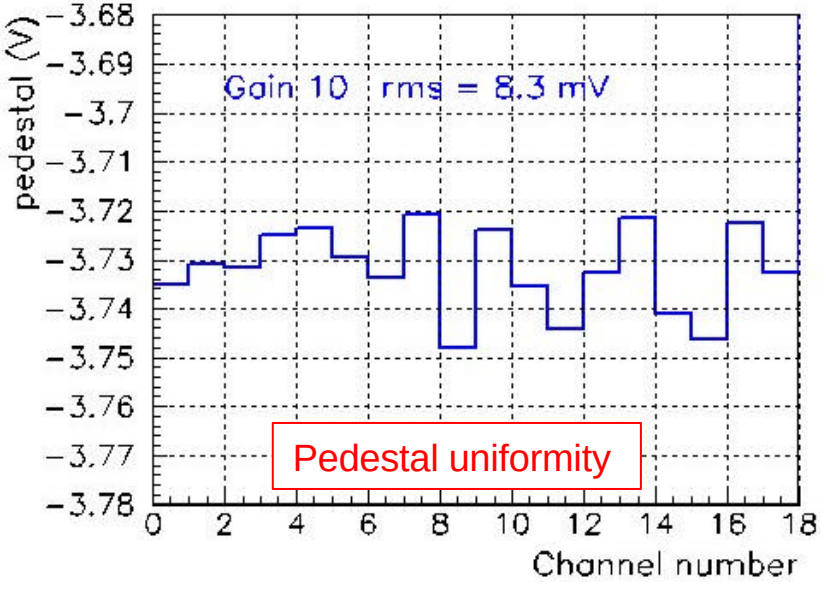


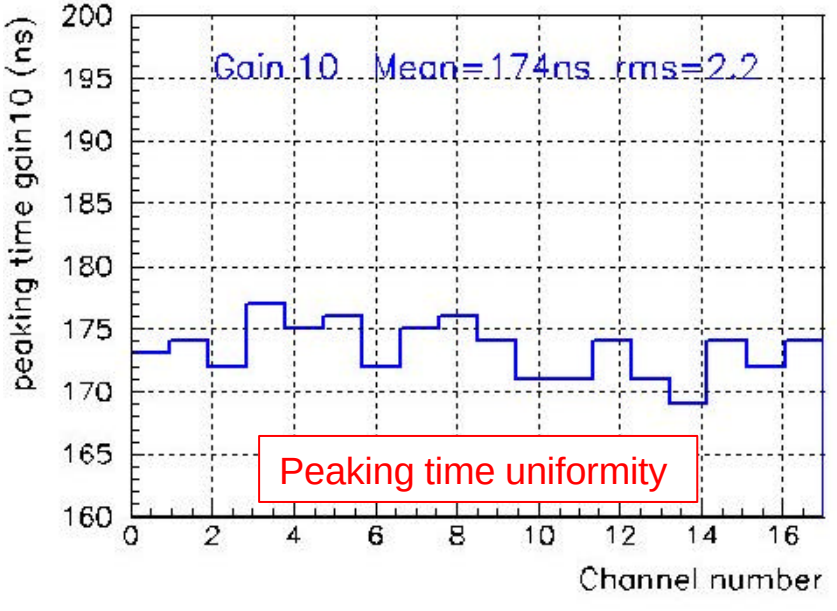


Signal uniformity (G10)

- **Signal (Gain 10, Cf=1.6pF)**
  - Amplitude = 3147 mV/pC ± 94
  - Peaking time = 174 ns ± 2 ns
  - Pedestals = -3.74 V ± 8.3 mV rms
- **Noise**
  - Cd = 0 pF : Vn = 500 µV
  - Cd = 68pF : Vn = 1.6 mV
- **Crosstalk**
  - < 0.2%



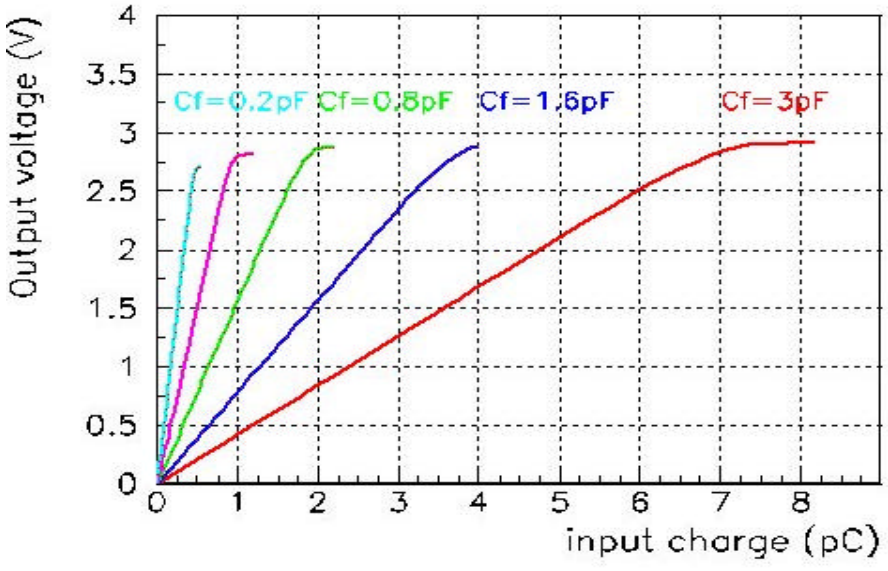


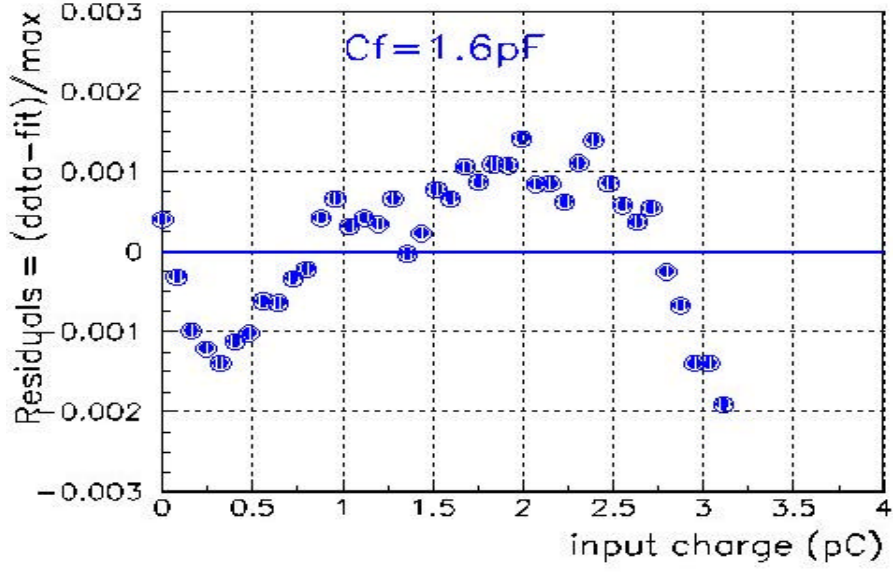


Linearity

- **Measured on all preamp gains**
  - Cf = 0.2, 0.4, 0.8, 1.6, 3 pF
  - Well within ± 0.2 %

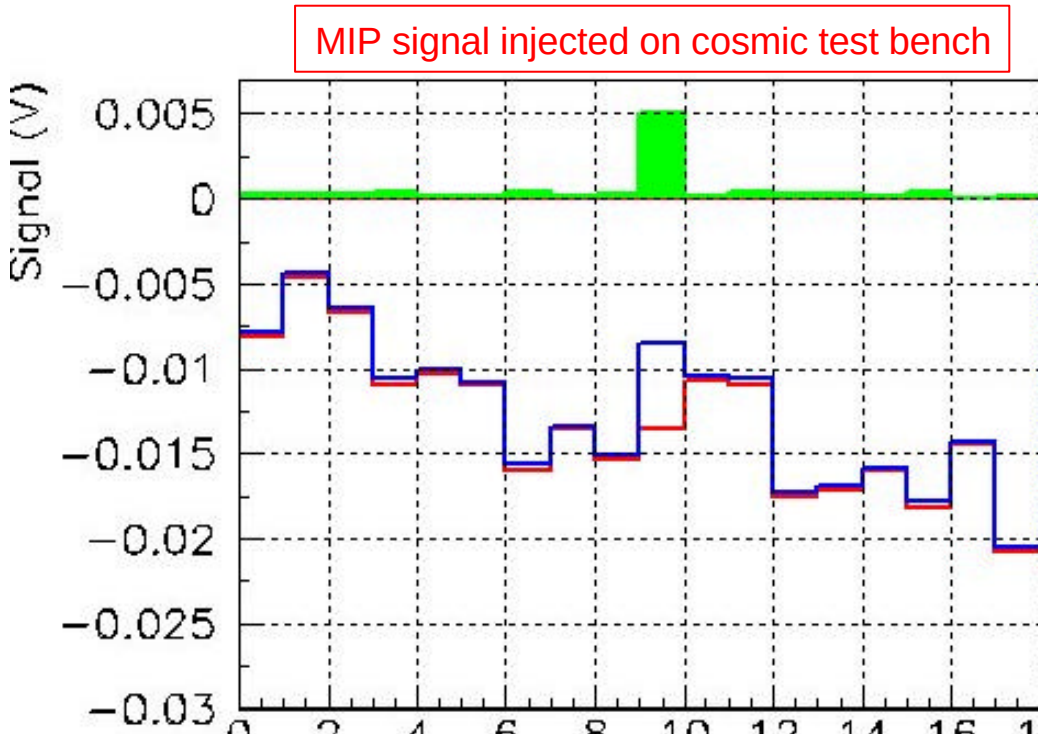
- **Dynamic range** (G1, C_f=1.6pF)
  - Max output : 3 V
  - linear (0.1%) range : 2.5V
    = 500 MIPS @ C_f = 1.6 pF
  - Noise :
    - 200 µV (Cd = 0)
    - 410 µV (Cd = 68pF)
    - **= 0.1 MIP @ C_d = 68 pF**
  - Dynamic range : **> 12 bits**
    - 13 000 (14 bits) @ Cd = 0
    - 6500 (12 bits) @ Cd = 68 pF
  - Can be easily extended by using the bi-gain outputs





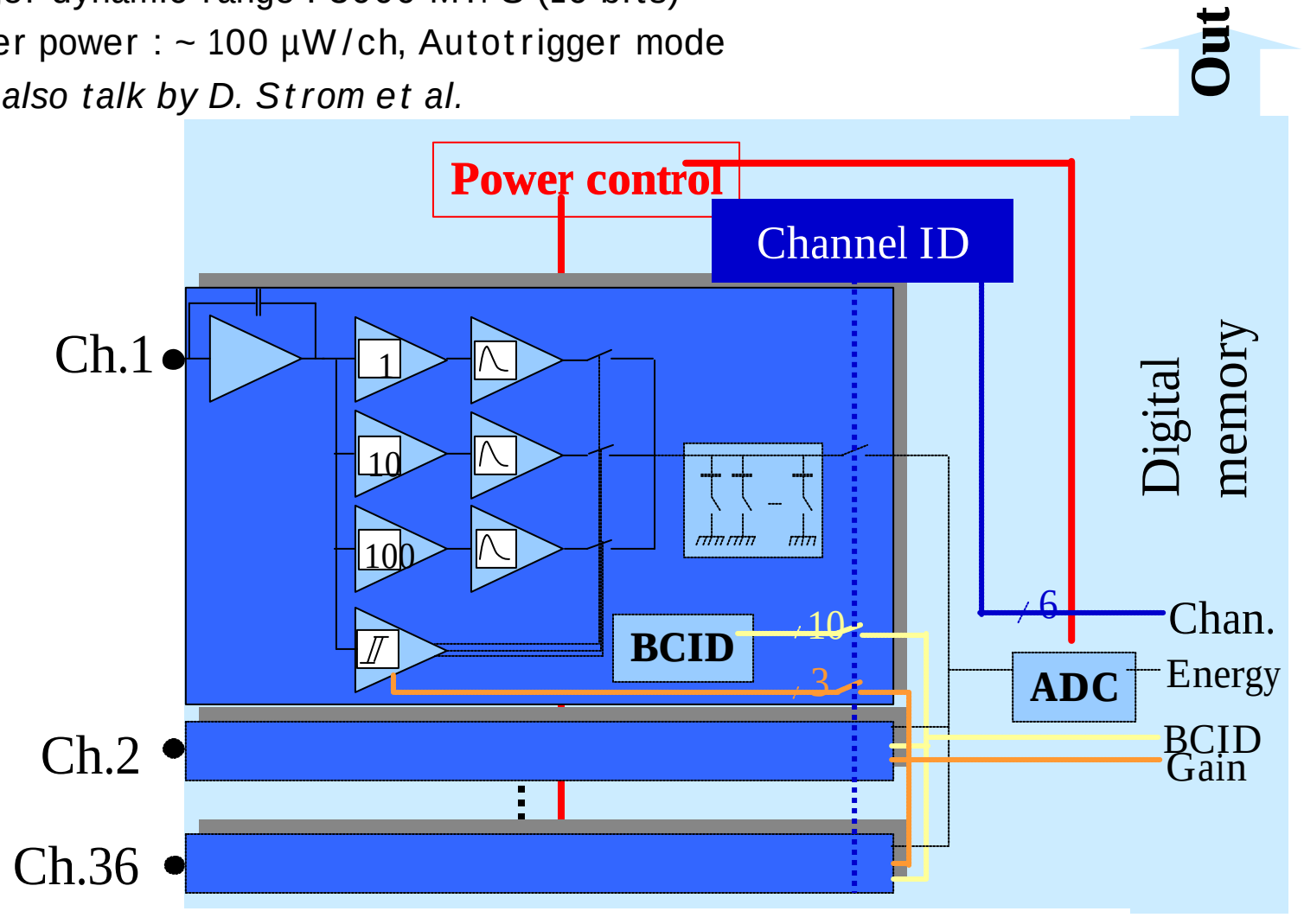
Results with detector

- **Cosmic test bench at LLR**
  - 1 MIP injected in channel 9
  - Calculation : 4.97 mV
  - Measurement : 5.05 mV
  - Well visible above the noise
- **MIP signal with ^{90}Sr source**
  - *See talk by J.C. Brient*
- **Readout boards**
  - Developed by UK group
    [P. Dauncey Imperial college]



Next steps

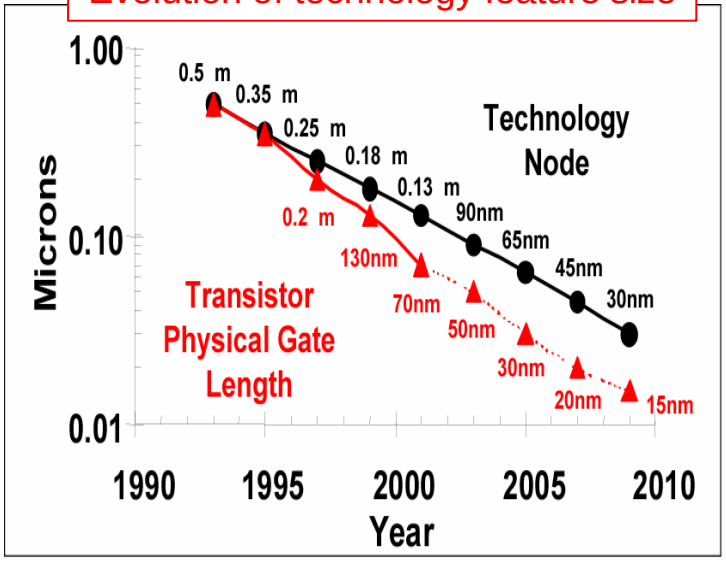
- **R&D on technological prototype**
  - Larger dynamic range : 3000 MIPS (16 bits)
  - Lower power : ~ 100 µW/ch, Autotrigger mode
  - *See also talk by D. Strom et al.*



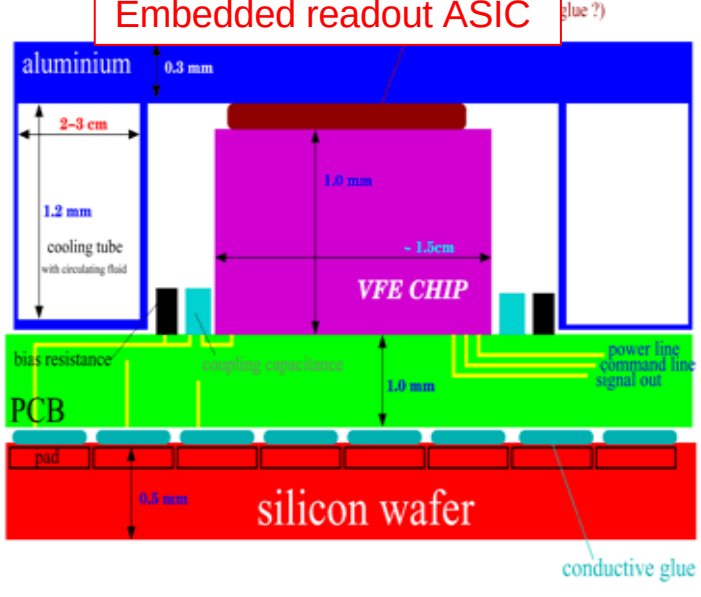
Next steps : technological prototype

- **Pending questions**
  - What technology to target for 2010-2020?
  - What about signal integrity on a 16bit mixed-signal chip ?
  - When to digitize ? Can we have 1 ADC /channel ?
  - What (low) power level can be reached ?

Evolution of technology feature size



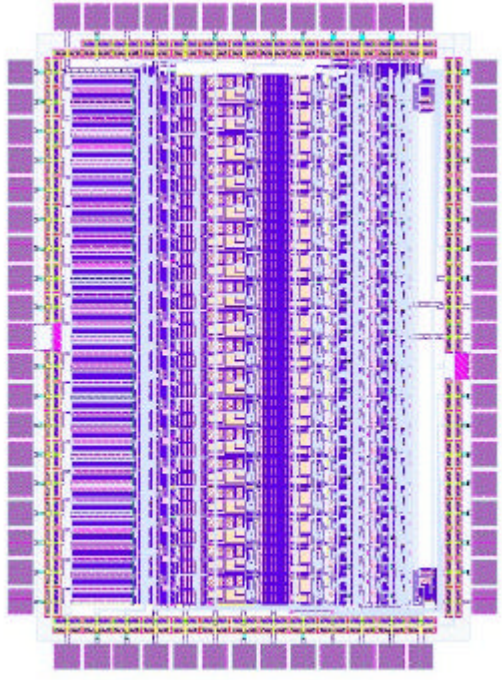
Embedded readout ASIC



Signal integrity on mixed-signal ASICs

Conclusion

- **FLCPHY3 chip fulfills FLC Wsi testbeam prototype**
  - Low Noise : 4000e- = 0.1 MIP
  - Maximum signal : 600 MIPs
  - Linearity : 0.1%, crosstalk 0.1%
  - Low pedestal dispersion : 4.8mV rms = 1 MIP
  - Can fit other detectors (variable gain 0.2-3pF, bi-gain G1-G10 shaper)



- **1000 chips have been produced for 2004-2005 testbeam**

- **Next steps**
  - Low power developments for technological prototype
  - New chip in SiGe 0.35µm with Idle mode
  - Trying to integrate the ADC…